APPLICATION NO. 10643375

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Claim 1 (currently amended): A semiconductor package having conductive bumps on a chip, comprising:

at least one chip having an active surface and an opposite inactive surface, and having a plurality of bond pads formed on the active surface;

a plurality of conductive bumps respectively formed on the bond pads of the chip;

~~an~~ a single encapsulation body for completely encapsulating the chip and the conductive bumps, wherein ends of the conductive bumps are exposed outside of the encapsulation body and flush with a surface of the encapsulation body;

a plurality of first conductive traces formed ~~on~~ at the surface of the encapsulation body exposing the conductive bumps and electrically connected to the exposed ends of the conductive bumps;

a solder mask layer applied over the first conductive traces and having a plurality of openings for exposing predetermined portions of the first conductive traces; and

a plurality of solder balls respectively formed on the exposed portions of the first conductive traces.

Claim 2 (original): The semiconductor package of claim 1, further comprising: at least one dielectric layer and a plurality of second conductive traces formed on the dielectric layer, the dielectric layer and the second conductive traces interposed between the first conductive traces and the solder mask layer, wherein the dielectric layer is located on the first conductive traces and has a plurality of vias by which the predetermined portions of the first conductive traces are exposed and electrically connected to the second conductive traces, and the solder mask layer is located on the second conductive traces whose predetermined portions are exposed via the openings of the solder mask layer and respectively connected to the plurality of solder balls.

Claim 3 (original): The semiconductor package of claim 1, wherein the inactive surface of the chip is exposed outside of the encapsulation body.

Claim 4 (original): The semiconductor package of claim 2, wherein the inactive surface of the chip is exposed outside of the encapsulation body.

Claim 5 (original): The semiconductor package of claim 1, wherein the conductive bump is selected from the group consisting of solder bump, high lead solder bump, gold bump, and gold stud bump.

Claim 6 (original): The semiconductor package of claim 2 wherein the conductive bump is selected from the group consisting of solder bump, high lead solder bump, gold bump, and gold stud bump.

Claim 7 (original): The semiconductor package of claim 1, wherein the exposed portions of the first conductive traces are terminals.

Claim 8 (original): The semiconductor package of claim 2, wherein the exposed portions of the second conductive traces are terminals.

CLAIMS 9-20 (CANCELLED)